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Total Number of Pages in This Submission		Attorney Docket Number	X-865-1D US
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Information Disclosure Statement (Supplemental)	Power Chang Addres	of Attorney, Revocation e of Correspondence ss	Copy of three (3) references

Substitute PTO-1449(s) IDS by Applicant (PTO/SB/08A) Request for Refund Certified Copy of Priority Document(s) Remarks Response to Missing Parts/ Incomplete Application Response to Missing Parts under 37 CFR 1.52 or 1.53 SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT Firm or Customer Number 24309 Lois D. Cartier (Customer Number) Reg. Number 40,941 Attn: Signature Charge any additional fees required/credit any overpayment to our Deposit Account Number: 24-0040 March 9, 2004 24-0040

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PATENT

IN THE UNITED STATES PATENT OFFICE

bplicants:

Michael J. Hart et al.

Assignee:

Xilinx, Inc.

Title:

"Structures and Methods for Selectively Applying a

Well Bias to Portions of a Programmable Device"

Serial No.:

10/624,617

File Date:

07-21-03

Examiner:

Unknown

Art Unit:

2819

2010

Docket No.:

X-865-1D US

Conf. No.:

6598

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P.O. Box 1450

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicants bring to the attention of the Examiner the four (4) references listed in the attached Substitute for Form 1449A. A copy of the three publications is enclosed.

Pursuant to rule 37 CFR 1.97(e)(1), Applicants certify that "each item of information contained in (this) Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of (this) information disclosure statement."

Citation of the above documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Citation of the above documents shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above documents shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

Respectfully submitted,

Lois D. Cartier

Attorney for Applicants

Reg. No. 40,941

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First Named Inventor	Michael J. Hart			
Art Unit	2819			
Examiner Name	Unknown			
Attorney Docket Number	X-865-1D US			

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Examiner	Cite	Document Number	Publication Date	Name of Patentee or	Pages, Columns, Lines, Where
Initials *	No.'	Number - Kind Code (if known)	MM-DD-YYYY	Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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¹ Applicant's unique citation designation number (optional). ² See Kinds of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁵ Applicant is to place a check mark here if English language Translation is attached.

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OTHER NON PATENT LITERATURE DOCUMENTS				
Examiner Initials *	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²	
	· ·	Nose, K. et al.; "V _{TH} -hopping Scheme for 82% Power Saving in Low-Voltage Processors"; Proceedings of the IEEE 2001 Custom Integrated Circuits Conference; May 6-9, 2001; pp. 93-96.		
		Kuroda, T. et al.; "A 0.9 V 150 MHz 10 mW 4 mm2-D Discrete Cosine Transform Core Processor with Variable-Threshold-Voltage Scheme"; Solid-State Circuits Conference; 1996; Digest of Technical Papers; 42nd ISSCC; IEEE International; February 8, 1996; pp. 166-167, 437.		
:		Kuroda, T. et al.; "A High-Speed Low-Power 0.3/sp1 mu/m CMOS Gate Array with Variable Threshold Voltage (VT) Scheme"; Custom Integrated Circuits Conference; 1996; Proceedings of the IEEE 1996; May 5-8 1996; pp. 53-56.		
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